It is important to note that, referring to FIG. 5, the function performed by the combination of an NCO (508, 518, 528, 538) followed by a phase selector (610, 620, 630, 640, 650, 660) can be implemented by analog circuitry. The analog circuitry can be described as follows. Each of the filtered phase errors outputted from the loop filters (506, 516, 526, 536) would be inputted to a D/A converter to be converted to analog form. Each of the analog filtered phase errors would then be inputted to a voltage-controlled oscillator (VCO). The VCOs would produce the clock signals. The VCOs can be implemented with well-known analog techniques such as those using varactor diodes. This embodiment is shown in FIG. 5A.

In The Claims:

Please cancel claims 1 - 40.

Please amend claim 41, and add new claims 43 - 60 as follows:

41. (Amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals, the processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the timing recovery system comprising:

(a) a set of phase detectors generating phase errors for the corresponding sampling clock signals;

(b) a set of loop filters coupled to the corresponding phase detectors, the loop filters receiving the corresponding phase errors and generating filtered phase errors;

(c) a set of digital-to-analog (D/A) converters coupled to the loop filters, the D/A converters receiving the filtered phase errors and generating analog filtered phase errors; and

(d) a set of oscillators coupled to the corresponding D/A converters, the oscillators receiving the analog filtered phase errors and generating the sampling clock signals, wherein the sampling clock signals so generated are transmitted to respective subsystems.

42. (Unchanged) The timing recovery system of claim 41 wherein the oscillators comprise varactor diodes.

43. (New) The timing recovery system of claim 41 wherein the set of clock signals further comprises a receive clock signal and wherein each of the processing subsystems further comprises a digital section, the digital sections operating in accordance with the receive clock signal.

44. (New) The timing recovery system of claim 43 wherein the receive clock signal is related to one of the sampling clock signals.

45. (New) The timing recovery system of claim 44 further comprising a first adder and a receive clock phase selector, the first adder receiving one of the phase control signals and a receive clock offset and generating a phase shift value, the receive clock phase selector receiving the phase shift value and generating the receive clock signal.

46. (New) The timing recovery system of claim 45 wherein the phase shift value comprises a set of phase steps and wherein the receive clock phase selector receives the phase shift value in the form of consecutive phase steps.

47. (New) The timing recovery system of claim 41 wherein the set of clock signals further comprises a transmit clock signal and wherein each of the subsystems further comprises a transmit section, the transmit sections operating in accordance with the transmit clock signal.

48. (New) The timing recovery system of claim 47 further comprising a transmit clock phase selector, the transmit clock phase selector receiving a transmit clock offset and generating the transmit clock signal.

49. (New) The timing recovery system of claim 48 wherein the transmit clock offset is equal to zero.

50. (New) The timing recovery system of claim 47 wherein the transmit clock signal is related to one of the sampling clock signals.

51. (New) The timing recovery system of claim 50 further comprising a transmit clock phase selector, the transmit clock phase selector receiving one of the phase control signals and generating the transmit clock signal.

52. (New) The timing recovery system of claim 41 wherein each of the phase detectors receives a corresponding slicer error and a corresponding tentative decision from a decoding system.

53. (New) The timing recovery system of claim 52 wherein each of the phase detectors comprises a lattice structure, the lattice structure comprising two delay elements, two multipliers and an adder, the lattice structure generating a pre-cursor phase error by multiplying the corresponding tentative decision by a delayed version of the corresponding slicer error and generating a post-cursor phase error by multiplying the corresponding slicer error by a delayed version of the corresponding

tentative decision and combining the pre-cursor and post-cursor phase errors to produce the corresponding phase error.

54. (New) The timing recovery system of claim 53 wherein at least one of the phase detectors further receives an offset input from a control unit and wherein the associated lattice structure combines the pre-cursor, post-cursor phase errors and the offset input to produce the corresponding phase error.

55. (New) The timing recovery system of claim 41 wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a filtered phase error.

56. (New) The timing recovery system of claim 41 wherein at least one of the loop filters comprises a first filter for accumulating a number of consecutive values of one of the phase errors to produce a sum value, a second filter for integrating the sum value to produce an integral value and an adder for combining the sum value and the integral value to produce a filtered phase error.

57. (New) The timing recovery system of claim 56 wherein the second filter includes a multiplier for scaling the integrated sum value by a scale factor to produce the integral value.

58. (New) A method for generating a set of clock signals in a system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding set of input signals, the system comprising a set of subsystems, each of the subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, the method comprising the operations of:

(a) generating a phase error for each of the sampling clock signals from a corresponding phase detector using signals associated with a corresponding

plurality of input signals;

(b) inputting each of the phase errors to a corresponding loop filter;

(c) generating filtered phase errors from the corresponding loop filters;

(d) converting the filtered phase errors to analog filtered phase errors;

(e) inputting each of the analog filtered phase errors to a corresponding oscillator;

and

(f) generating sampling clock signals from the corresponding oscillators.

59. (New) A method for generating a set of clock signals in a system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals and a receive clock signal, the system comprising a set of subsystems, each of the subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the subsystems comprising a digital section, each of the digital sections operating in accordance with the receive clock signal, the method comprising the operations of:

(a) receiving a plurality of transmitted signals;

(b) generating phase control signals associated with each of the plurality of transmitted signals;

(c) generating a receive phase control signal for the receive clock signal in accordance with at least one of the phase control signals;

(d) generating the sampling clock signals in accordance with the corresponding phase control signals;

and

(e) generating the receive clock signal in accordance with the receive phase control signal.

60. (New) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals and a receive clock signal, the

processing system comprising a set of processing subsystems, each of the processing subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the processing subsystems comprising a digital section, each of the digital sections operating in accordance with the receive clock signal, the timing recovery system comprising:

(a) a decoder for generating a plurality of signals associated with the plurality of transmitted signals;

and

(b) a timing recovery circuit for receiving the signals generated by the decoder, and for generating phase control signals associated with each of the plurality of transmitted signals and a receive phase control signal for the receive clock signal in accordance with at least one of the phase control signals, wherein the timing recovery circuit generates the sampling clock signals in accordance with the corresponding phase control signals and generates the receive clock signal in accordance with the receive phase control signal.

A4 Cont.

REMARKS

In the parent application (Serial No. 09/437,721) claim 41 was rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Number 5,726,607 to Brede et al. and claim 42 was rejected under 35 U.S.C. §103(a) as being unpatentable over the Brede et al. patent in view of U.S. Patent Number 5,644,271 to Mollov et al.

By this Preliminary Amendment, claims 1-40 have been cancelled, claim 41 has been amended, new claims 43 - 60 have been added.

In addition, the specification has been amended to incorporate amendments made in the parent application and to update the CROSS-REFERENCE TO RELATED APPLICATIONS to refer to the parent application. No new matter has been added.

Reconsideration of rejected claims 41 and 42 is respectfully requested, in light of the above claim amendments and the following remarks. Amended claim 41 is